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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/735,555 | 12/14/2000 | Kunihiro Itoh | 108075-00022 | 6570 |

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| EXAMINER |
|---|
| CHANG, DANIEL D |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2819 | |

DATE MAILED: 11/01/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/735,555 | ITOH ET AL. | |
| | Examiner | Art Unit | |
| | Daniel D. Chang | 2819 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *29 August 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-11 and 19-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 19-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

### *Acknowledgement*

Receipt is acknowledged of the Amendment filed August 29, 2002.

### *Claim Objections*

Claim 23 is objected to because of the following informalities: on line 9, "generated" appears to be --generate--. Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1-11 and 19-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Wert et al. (US 6,281,706 B1).

Regarding claims 5-11, 21-22, and 25-27, Wert teaches, in figures 7A, 7B and 8, an output buffer circuit comprising:

a first drive circuit, connected to an output terminal (305), for receiving an input signal (301) and generating a first output signal (output of 701/711) having a first state (logic HIGH/LOW);

a second drive circuit connected to the output terminal and having a lower output impedance than the first drive circuit (inherent, see col. 3, lines 8-18, col. 4, 3-42), wherein the

second drive circuit generates a second output signal (output of 705/717) having the first state (logic HIGH/LOW); and

a first control circuit (707/719), connected to the second drive circuit, for generating a first control signal (725/726) for driving the second drive circuit on the basis of the input signal and the first output signal after the first output signal (output of 701/711) is changed by a predetermined amount (see Fig. 7B of Wert and attached figure A) by the first drive circuit.

Method claims 1-4, 19-20, and 23-24 are essentially the same in scope as apparatus claims 5-11, 21-22, and 25-27 and are rejected similarly.

***Response to Arguments***

Applicant's arguments filed August 29, 2002 have been fully considered but they are not persuasive.

Applicant argues, on page 9 of the amendment, that "Wert does not and cannot teach driving the second drive circuit after the output signal of the first drive circuit changes by a predetermined amount because the second drive circuit is automatically driven while the first drive circuit is driven". However, in response to a low to high transition of an input signal, Wert also teaches (col. 3, lines 54-67; col. 4, lines 20-34; and figure 7B) that the transistor 705 of the second drive circuit turns on after the transistor 701 of the first drive circuit turns on (see Fig. 7B of Wert and attached figure A). Transistors 711 and 717 are turned off at this time. When the transistor 701 turns on, the output signal of the first drive circuit (OUTPUT 305) will start changing from logic low to logic high (see A1 in attached figure A); and when the transistor 705 turns on, the output signal will stay high. Looking at the period from the point where the

transistor 701 turns on to the point where the transistor 705 turns on (A1 in attached figure A), the control signal is "driving the second drive circuit (to turn on 705 and turn off 717) on the basis of the input signal (301 via 310, 709, and 707) and the first output signal (output of 701 via 305 and 728) is changed by a predetermined amount (see attached figure A) by the first drive circuit.

As each and every limitation is found in the Wert reference, as explained above, the rejection of claims 1-11 and 19-27 as anticipated by Wert is maintained.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (703) 306-4549. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on (703) 305-3493. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Daniel D. Chang
Examiner
Art Unit 2819

DC
October 30, 2002

DANIEL CHANG
PRIMARY EXAMINER

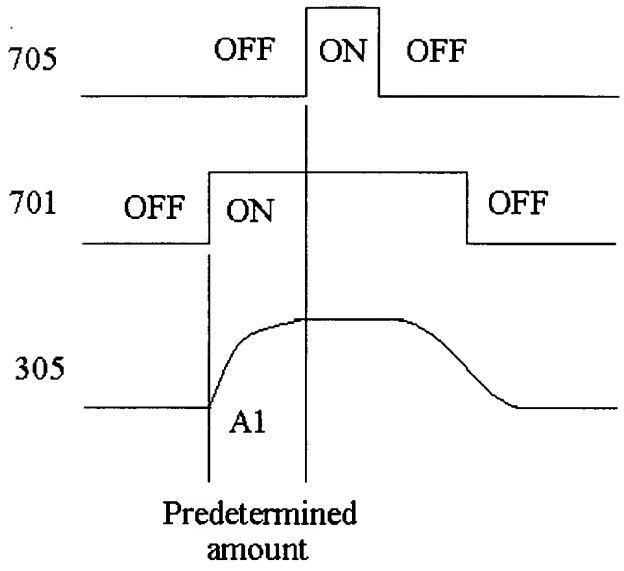


Figure A. Waveform of OUTPUT 305 based on the output of transistors 701 and 705 in Fig. 7A of US Pat. No. 6,281,706 B1. This figure is based on Fig. 7B of US Pat. No. 6,281,706 B1.